ANALYSIS AND DESIGN OF MICROSLAB™ WAVEGUIDE

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Abstract - Microslab™, a novel low-loss semi-planar waveguide, is studied to provide design charts for the propagation constant and characteristic impedance. A parallel-plate analysis is performed to provide design guidelines based on frequency, conductor loss, and size. A mode-matching procedure is then used to build the design charts. Results are provided for microslab implementation on GaAs substrates.

I. INTRODUCTION

Microslab™ waveguide was recently proposed to address the problem of conductor losses in millimeter-wave waveguides [1] (see Fig.1). In order to design components in microslab, information of engineering utility is required for the loss, propagation constant, and characteristic impedance of the dominant mode [2] along with the propagation constant of the first higher order mode. Useful results to date include only an approximate closed-form formula for the impedance [3].

This paper presents the information necessary to design microslab lines on GaAs substrates by using a mode-matching analysis to construct design charts. Mode-matching is a very computationally intensive solution technique which becomes even more so for complicated structures. Numerical optimization to minimize the conductor loss is not feasible. To reduce the problem, a thin strip approximation will be used; however, this approximation precludes the calculation of the conductor loss [4]. In order to design microslab structures for minimum conductor loss, the parallel-plate waveguide is analysed for the conductor loss and optimized to provide design charts from which microslab dimensions can be chosen. In this way, the loss is optimized in an approximate manner while reducing the computional load of the mode-matching analysis. With these dimensions, the mode-matching analysis is applied for several strip widths to build design charts for the propagation constant and characteristic impedance.

II. PARALLEL-PLATE ANALYSIS

For high frequencies and/or wide strips, microslab operation is similar to the dielectric layered parallel-plate waveguide shown in Fig.2. Conductor losses can be reduced by reducing the tangential magnetic field strength at the conductors. For the structure in Fig.2, this can be accomplished by selecting $\varepsilon_2>\varepsilon_1,\varepsilon_3$ and operating the waveguide at a frequency such that $(\beta/\beta o)^2>\varepsilon_1,\varepsilon_3$, which will induce decaying fields in the ε_1 and ε_3 layers. Increasing the frequency further reduces the loss due to the increased decay rate in the fields. However, it is well known that for such structures the dominant mode switches types from TM^y at low frquencies to TE^y at high frequencies [5,6]. The physical reason for this phenomena is that TM^y operation is induced at low frequencies by the presence of two conductors. At high frequencies, the fields decay and do not see the conductors, resulting in an asymmetric slab as the effective waveguide, for which the dominant mode is always TE^y [7]. Therefore, the dispersion curves for the two modes must cross at some frequency, f_s. Since operation in the TE^y mode is undesirable due to the unfavorable field configuration, the operation frequency is bounded above by f_s, where the loss is minimum. For microslab, the $E_{11}{}^y$ mode is dominant at low frequencies, and the $E_{11}{}^x$ is dominant at high frequencies.

Both the parallel-plate optimization and the mode-matching analysis require the calculation of the modes of the parallel-plate waveguide. The fields can be generally described in terms of scalar potentials [8], and application of the appropriate boundary conditions yields the eigenvalue equations for the guided modes. The conductor losses for the TM^y mode are given by

$$\alpha_c=R_s\int_c|H_t|^2dl/(2Re\int_s(\mathbf{E}\times\mathbf{H}^*)\cdot\hat{\mathbf{z}}ds)$$

$$=[\omega R_s/(2k_z)]\,[\phi^2(c)+\phi^2(0)]/\int_0^c\phi^2(y)/\varepsilon(y)\,dy$$

where $R_s=2.61\times10^{-7}f^{0.5}\ \Omega$ for copper, and $\phi(y)$ is the TM^y scalar potential.

To build the parallel-plate design curves, the TM^y and TE^y eigenvalue equations are optimized by varying the structure dimensions to provide for dispersion curve intersection at a given f_s. The structure is symmetric with $a=(c-b)=\gamma(b-a)$ and $\varepsilon_1=\varepsilon_3$, where γ is the dimensionless optimization variable. The resulting curves of Fig.3 plot the proper structure dimensions to achieve intersection at f_s, the conductor losses for copper at $0.6f_s$, $0.8f_s$, and $1.0f_s$, and the propagation constant at f_s as a function of γ.

Several observations can be made concerning the plots. The dominant features are a minimum in the overall structure size [since $c=(2\gamma+1)x(b-a)$], a peak in the conductor loss, and increasing conductor loss with decreasing frequency (an intuitive result). These features contradict, resulting in design tradeoffs between loss and size, and loss and higher order modes.

III. MODE-MATCHING ANALYSIS

The mode-matching procedure used is an extension of the method used by Mittra, et.al. [9] to include the bifurcation

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introduced by the center strip metallization. The structure can be modified to simplify the formulation. Lateral symmetry is exploited to divide the structure along the x=0 plane, thereby reducing the problem by half. A magnetic wall at the x=0 plane eliminates the odd modes, while an electric wall eliminates the even modes. The resulting structure is subdivided for modal expansion as shown in Fig.4. Note that the formulation process below y=c is identical to that above. The formulation details for the either are available in [9].

The specific implementaion details concern the number of retained expansion terms, the dielectric composition of each region, and the variable type used in the computation. For computer implementation, the expansions are truncated at M, N, and L terms in regions 1, 2, and 3, respectively. We retain an equal number of TM^y and TE^y modes so that the total number of terms in each region is 2M, 2N, and 2L. There are two requirements on the number of expansion terms retained: a square matrix requires that M+N=L, and matching the spectral components along the regional interface require that M/N=c/(d-c). One expansion coefficient is chosen to select the accuracy of the solution. The specific dielectrics implemented are shown in Fig.5, where the ε_5 dielectric layer was added to the basic microslab structure to facilitate checking the program. Finally, the problem is formulated entirely in real functions and only real solutions are searched and computed. This limits the search to non-leaky solutions (of primary interest), but it greatly reduces the computation time.

The definition implemented for the characteristic impedance calculation is dictated by the behavior of the current on the center strip metallization. Since the fields connect with the strip metallization via evanescent fields, the induced current is small. As the frequency increases, the fields decay more rapidly and even smaller currents are produced. As $f \rightarrow \infty$, then $I \rightarrow 0$. Consequently, $Z_0=P/(II^*) \rightarrow \infty$ and $Z_0=V/I \rightarrow \infty$. This undesirable behavior is not found in the power-voltage definition; therefore, it will be used here. The integration path for the voltage is taken from 0 to c along x=0 in Fig.4.

IV. DESIGN TRADEOFFS

This section investigates microslab operation so that a set of guidelines for the design of microslab can be determined. The parallel-plate analysis of Section II provides guidelines for selecting structure dimensions as a function of γ (see Fig.3). In this section, the effect of γ on microslab operation is investigated.

Several microslab structures were designed using the chart in Fig.3(b) using γ values of 0.25, 0.63, and 1.59. The structures were analysed with the mode-matching analysis of Section III, and since exact answers were not required, we chose d=2c and M=6. For all cases we chose g=c/4 in order to obtain similar modes of operation. The dispersion curves appear in Fig.6. Modes with effective dielectric constants at and below the dashed curve are leaky. From this figure and the discussion in Section II on parallel-plate waveguide tradeoffs, the design tradeoffs in Table I are deduced. In this table, γ_0 is defined as the γ for which the minimum structure size is realized.

V. DESIGN CHARTS

Design charts for the propagation constant and characteristic impedance of microslab lines on GaAs substrates are presented in this section. The dimensions were chosen from the charts in Fig.3 and the tradeoffs in Table I. Three specific implementations corresponding to the three charts in Fig.3 are presented in Figs. 7, 8, and 9. The dispersion curves are plotted only where a single non-leaky mode exits. Below the dashed line, leaky modes may exist.

Characteristic	decreasing $\gamma<\gamma_0$	increasing $\gamma>\gamma_0$
Dispersion	decreases	decreases
Decay Rate	decreases	decreases
Impedance	improves	worsens
Higher Order Modes	increases	decreases
Size	increases	increases
Loss	decreases	increases†

Table 1. Microslab design tradeoffs.
† Increases over the range of interest.

Convergence tests are performed for a thin strip at the lowest frequency of the design chart, where convergence is slowest. The first solution to fall within ±0.5% in propagation constant and ±1.5% in impedance of the estimated convergent value is accepted.

The height "d" selected for the coverplate is of considerable importance. Since region 2 of Fig.4 contains a homogeneous dielectric, the fields in the region will always be sinusoidal in nature in the y-direction. Since the computation time greatly increases as the plate height increases, it is not possible to simulate the open microslab case. Instead, we place the coverplate at a half free space wavelength above the center strip metallization at the lowest frequency of the design curve. The plate remains at this height for all frequencies. The plate height is reduced if there is a negligible (<<1%) effect.

The design charts show similar features. The dispersion curves demonstrate the expected behavior where the effective dielectric constant increases with increasing width. The impedance curves are more complicated. At low frequencies, the fields penetrate the insulating dielectrics and microslab behaves like microstip: impedance increases with frequency and decreases with strip width. At high frequencies, the fields do not penetrate the insulating dielectrics as well, and the impedance exhibits behavior derived from both microslab and parallel-plate operation. The resulting behavior is unintuitive and quite complex.

ACKNOWLEDGMENT

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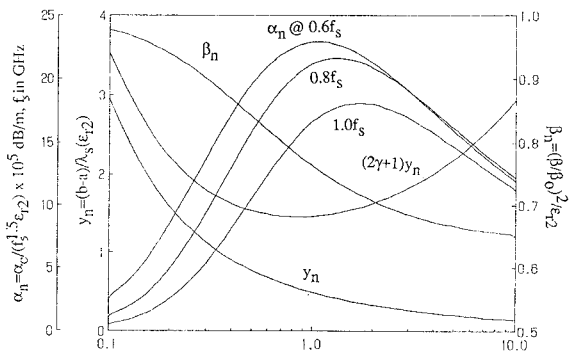
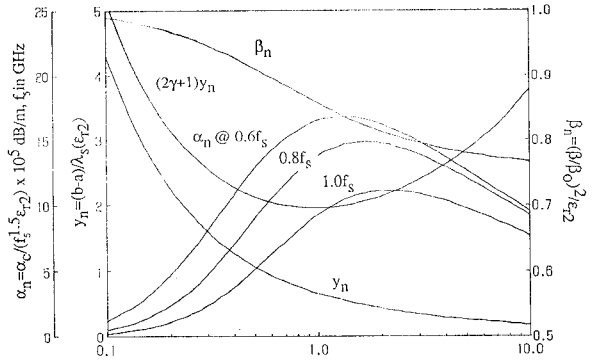
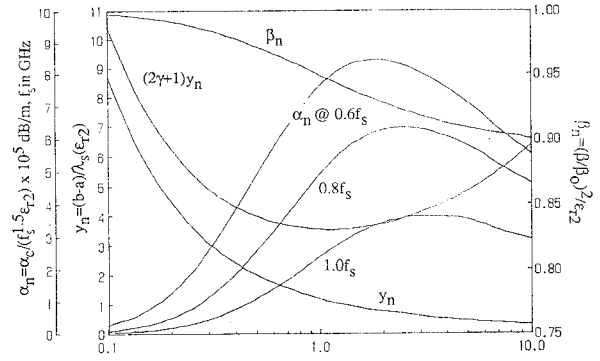


(a) $\varepsilon_1=\varepsilon_3=0.6357\varepsilon_2$



(b) $\varepsilon_1=\varepsilon_3=0.7519\varepsilon_2$



(c) $\varepsilon_1=\varepsilon_3=0.8915\varepsilon_2$.

Fig.3. Optimized parameters for the parallel-plate waveguide for intersection of the TM^y and TE^y mode dispersion curves at a frequency f_s.

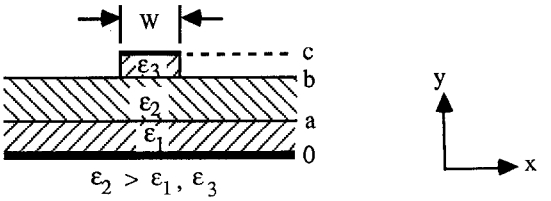


Fig.1. Microslab waveguide.

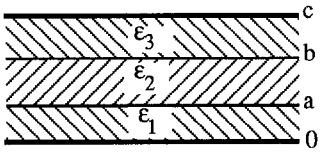


Fig.2. Parallel-plate waveguide model for microslab.

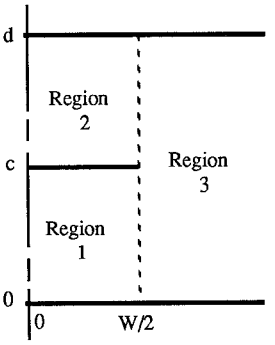


Fig.4. Subdivision for analysis.

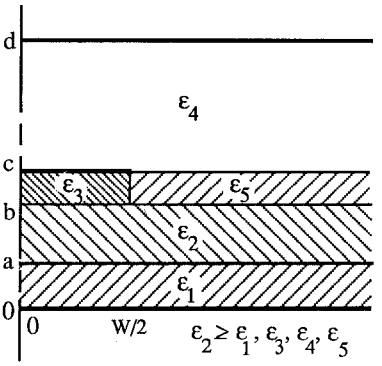


Fig.5. Dielectrics used in implemented solution.

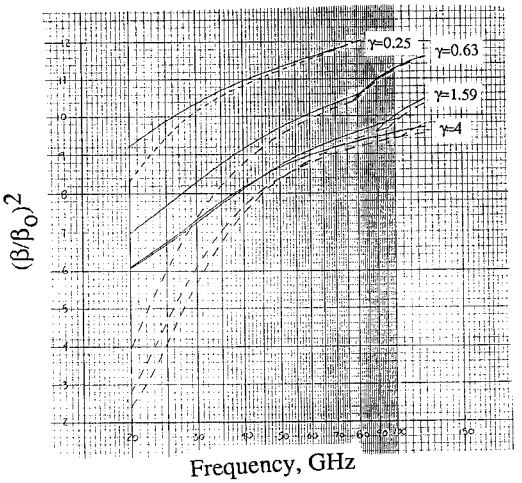


Fig.6. Microslab dispersion results for several γ.

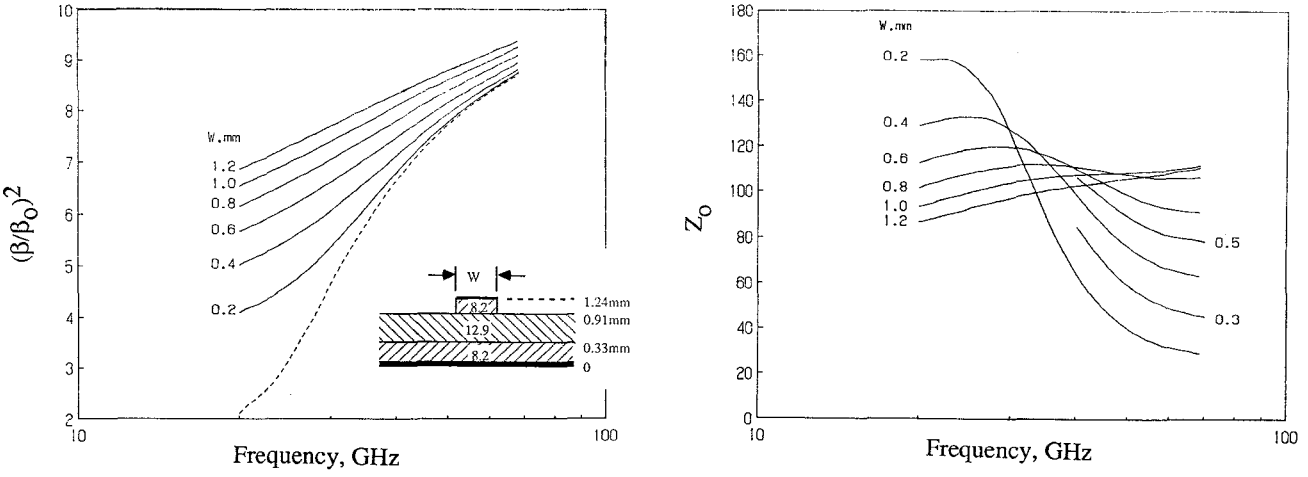


Fig.7. Microslab design charts for $\varepsilon_{r1}=\varepsilon_{r3}=8.2$ and $\varepsilon_{r2}=12.9$.

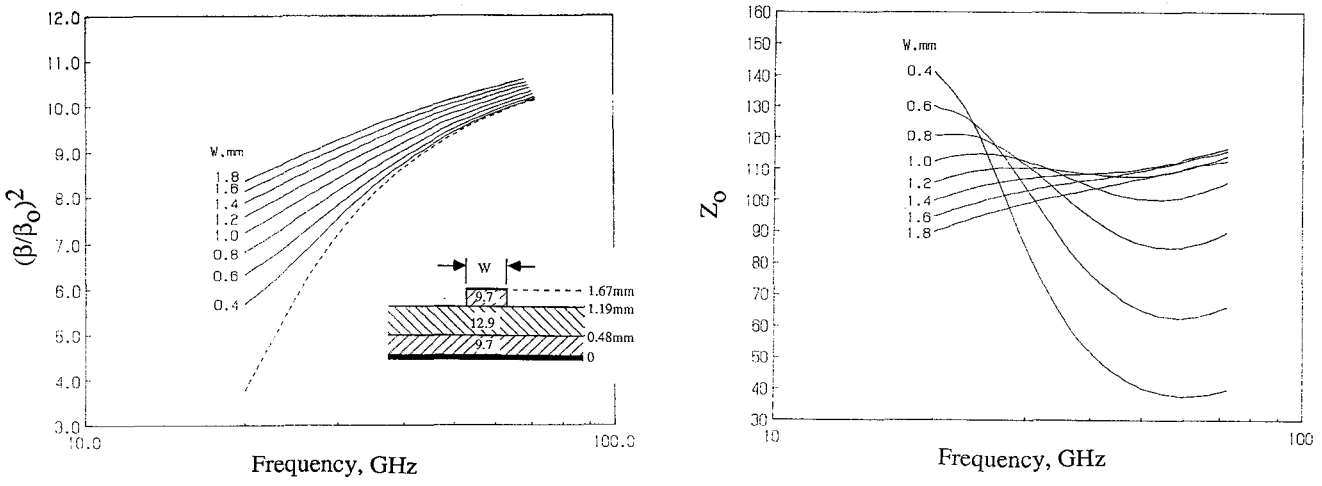


Fig.8. Microslab design charts for $\varepsilon_{r1}=\varepsilon_{r3}=9.7$ and $\varepsilon_{r2}=12.9$.

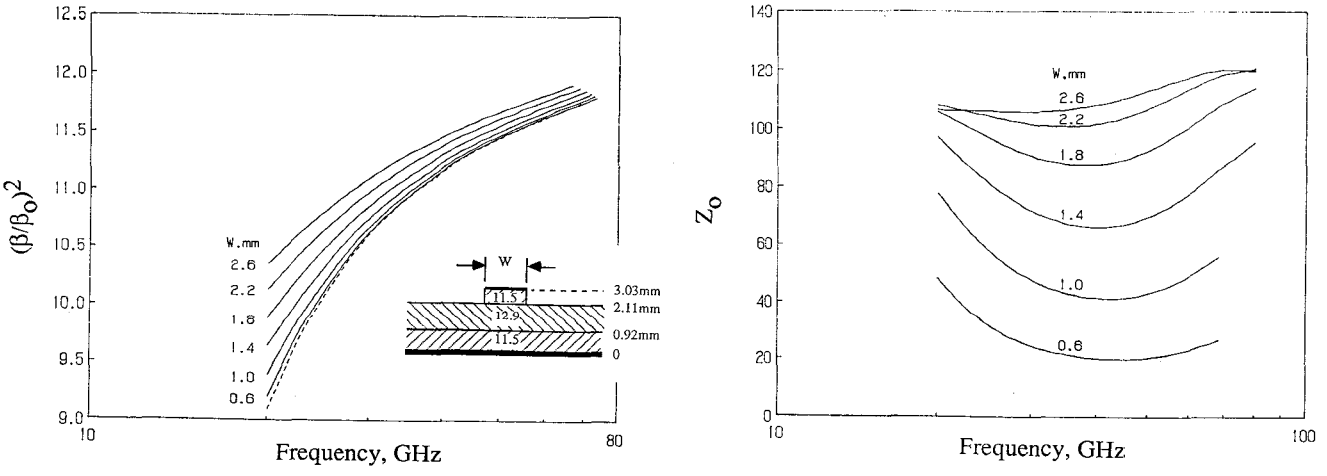


Fig.9.Microslab design charts for $\varepsilon_{r1}=\varepsilon_{r3}=11.5$ and $\varepsilon_{r2}=12.9$.